UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,776	06/26/2003	Luc Burgun	02935.000001.	4879

5514 7590 06/20/2008

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

MAIL DATE	DELIVERY MODE
06/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,776	BURGUN ET AL.	
	Examiner	Art Unit	
	SAIF A. ALHIJA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

10603776

DETAILED ACTION

1. Claims 1-25 have been presented for examination.

Response to Arguments

2. Applicant's arguments filed 19 March 2008 have been fully considered but they are not persuasive.

PRIOR ART ARGUMENTS

i) Applicants argue that Lin does not teach "reconfigurable circuits" to be part of the RCC computing system. The Examiner first notes that claim 1 does not contain the phrase "reconfigurable circuit" but rather recites a "reconfigurable hardware part." Applicants argued terminology does not appear until the recitation by claim 10 that the "reconfigurable test bench comprises a fixed part and at least one **reconfigurable interface circuit** embodying the emulated part of the test environment." Second, the Examiner notes that Applicants are using extremely broad terminology in an attempt to define a specific term. The Examiners assertion is supported by Applicants statements that the reconfigurable circuits are for example an FPGA manufactured by Xilinx, see page 11 second paragraph of their remarks. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., reconfigurable circuit being an FPGA) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Examiner further notes that based on the broadest most reasonable interpretation of "reconfigurable hardware part" and "reconfigurable interface circuit" the RCC computing system reads on the present invention since the computing system contains reconfigurable test bench's, drivers, and models which reconfigure the hardware/interface circuit of the RCC computing system as can be seen in Figure 69 where the reconfigurable elements include elements 2143-2144, as well as the reconfigurable I/O components of the RCC computing system see Column 11, Lines 16-34, as well as the PCI bus connection which is reconfigurable in the sense that the PCI connects the RCC computing system to element 2154 which is an external memory buffer which as per Column 129 Line 65-Column 130, Line 5 can be reconfigured to allow different types of device memory storage for the RCC computing system, which is directed at the term "reconfigurable interface circuit" recited in the claims. The Examiner appreciates the Applicants arguments and amendments to clarify Applicants claimed

invention and respectfully recommends that Applicants include the specificity of their arguments, such as a specific definition of the broad terms reconfigurable hardware parts and interface circuits, into the claim language since the Examiner must take the broadest most reasonable interpretation of the claims when determining the relevance of prior art.

EXAMINERS NOTES

ii) Examiner has cited particular columns and line numbers in the references applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

iii) The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution.

iv) Further, the Examiner respectfully encourages Applicants to direct the specificity of their response with regards to this office action to the broadest reasonable interpretation of the claims as presented. This will avoid issues that would delay prosecution such as limitations not explicitly presented in the claims, intended use statements that carry no patentable weight, mere allegations of patentability, and novelty that is not clearly expressed.

v) The Examiner also respectfully requests Applicants, in the event they choose to amend, to supply a clean version of the presented claims in addition to the marked-up copy in order to avoid potential inaccuracies with the version of the claims that would be examined.

PRIORITY

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in France on 26 June 2002. It is noted, however, that applicant has not yet filed a certified copy of the 0207949 application as required by 35 U.S.C. 119(b). Appropriate correction is required.

Claim Rejections – 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by **Lin et al. "Coverification System and Method", U.S. Patent No. 6,389,379,** hereafter referred to as **Lin.**

Regarding Claim 1:

Lin discloses Method of emulating a design under test associated with a test environment, the method comprising

generating in a first phase a first file representative of a synthesizable portion of the test environment, and **(Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

generating in a second phase a second file representative of at least a part of the design under test, **(Abstract. Figures 10, 16, and 67, for example, and their corresponding descriptions.)**

delivering the first configuration file to a first reconfigurable hardware part forming a reconfigurable test bench so as to emulate the synthesizable portion of the test environment, **(Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)** and

delivering the second configuration file to a second reconfigurable hardware part so as to emulate the design under test, **(Abstract. Figures 1-6, and their corresponding descriptions.)**

performing simulation, using the reconfigurable test bench to produce emulation results, **(Column 1, Lines 10-15)**

wherein the first and second reconfigurable hardware parts are distinct and mutually connected. **(Abstract. Figure 67 and corresponding descriptions.)**

Regarding Claim 2:

Lin discloses Method according to claim 1, the first phase comprises

producing a logic circuit comprising a network of logic gates, the logic circuit being representative of the synthesizable portion of the test environment and compilation directives, **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)** and

compiling the logic circuit in accordance with said directives, so as to obtain the first configuration file. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 3:

Lin discloses Method according to claim 2, wherein the test environment comprises a collection of drivers and monitors and the production of the logic circuit comprises the formation of hardware blocks in the form of networks of logic gates, these hardware blocks representing interfaces of drivers/monitors of software stimulation, interfaces of drivers/monitors of real hardware stimulation, drivers/monitors of emulated hardware stimulation, blocks for calculations of hardware triggers, and a block for interfacing with the emulator of the design under test. **(Figures 28-30 and their corresponding descriptions)**

Regarding Claim 4:

Lin discloses Method according to claim 3, wherein the formation of the hardware blocks is effected on the basis of statically defined networks of gates or of networks of gates which are generated dynamically by a software module. **(Column 8, Line 21 – Column 9, Line 19)**

Regarding Claim 5:

Lin discloses Method according to any one of claims 1 to 4, wherein the first phase and the second phase are performed in parallel. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding**

descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)

Regarding Claim 6:

Lin discloses Method according to any one of claims 1 to 4, wherein the first phase and the second phase are performed sequentially. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 7:

Lin discloses Method according to claim 6, wherein the first phase is performed before or after the second phase. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 8:

Lin discloses Method according to claim 3, wherein

when the first phase is performed after the second phase, the production of the logic circuit uses as input parameters a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, and

when the second phase is performed after the first phase, the production of the logic circuit uses as input parameters a description of the interface of the design under test and supplies as output a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, the output description being used as a constraint parameter for the second phase. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 9:

Lin discloses Emulation system for emulating a design under test associated with a test environment, the system comprising

a host computer, **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

a reconfigurable hardware test bench connected to the host computer and operable to emulate a synthesizable portion of the test environment, **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

a reconfigurable hardware emulator, connected to and distinct from the test bench, and operable to emulate the design under test, **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

first generating means operable to generate a first file representative of the test environment, **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)** and

second generating means operable to generate a second file representative of the design under test. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 10:

Lin discloses System according to claim 9, wherein the reconfigurable test bench comprises a fixed part and at least one reconfigurable interface circuit embodying the emulated part of the test environment. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 11:

Lin discloses System according to claim 10, wherein the fixed part comprises at least one control circuit and one circuit for interfacing with the host computer, and in that the reconfigurable interface circuit comprises interfaces of drivers/monitors of software stimulation which are operable to establish communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation. **(Figures 28-30 and their corresponding descriptions)**

Regarding Claim 12:

Lin discloses System according to claim 11, wherein the fixed part furthermore comprises hardware drivers/monitors, and the reconfigurable circuit comprises interfaces with the hardware drivers/monitors. **(Figures 28-30 and their corresponding descriptions)**

Regarding Claim 13:

Lin discloses System according to any one of claims 9 to 12, wherein the fixed part comprises a circuit for interfacing with a target device. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 14:

Lin discloses System according to claim 9, wherein the fixed part comprises a control part of a hardware logic analyser whose state evolves as a function of the hardware triggers. **(Column 9, Line 33-58)**

Regarding Claim 15:

Lin discloses System according to claim 9, wherein the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals synchronizing the emulator of the design under test and certain at least of the hardware means of the test bench, the reconfigurable test bench further comprising clock retrocontrol means operable to in response to at least one wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal temporarily disable certain of the other secondary clock signals with different frequencies from that of the first secondary clock signal. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 16:

Lin discloses System according to claim 9, wherein the test bench and the emulator are embodied on an electronic card external to the host computer and connected to a mother card of the host computer. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 17:

Lin discloses System according to claim 9, wherein the reconfigurable test bench is embodied on a first electronic card external to the host computer and connected to a mother card of the host computer, and the emulator of the design under test is embodied on one or more other cards external to the host computer and connected to the first electronic card. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 18:

Lin discloses System according to claim 17, wherein the circuit for interfacing with the target device is integrated into the first electronic card. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 19:

Lin discloses System according to any one of claims 10 to 12, wherein the test bench and the emulator are embodied on an internal electronic card (CINT) incorporated into the host computer. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 20:

Lin discloses System according to claim 13, wherein the circuit for interfacing with the target device is embodied on an external electronic card outside the host computer, and configured to be connected to the internal electronic card. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions.**

Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)

Regarding Claim 21:

Lin discloses An apparatus in the form of an electronic card, configured to be connected to the mother card of a host computer, the electronic card comprising

a reconfigurable hardware test bench operable to emulate a synthesizable portion of a test environment associated with a design under test, and

a reconfigurable hardware emulator, distinct from the test bench, connected to the reconfigurable test bench and operable to emulate the design under test. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 22:

Lin discloses The apparatus according to claim 21, wherein the reconfigurable test bench comprises a fixed part and at least one reconfigurable circuit operable to embody the emulated part of the test environment. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 23:

Lin discloses The apparatus according to claim 22, wherein the fixed part comprises at least one control circuit and one circuit for interfacing with the host computer, and the reconfigurable circuit comprises interfaces of drivers/monitors of software stimulation which are operable to establish a communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation. **(Figures 28-30 and their corresponding descriptions)**

Regarding Claim 24:

Lin discloses The apparatus according to claim 23, wherein the fixed part furthermore comprises hardware drivers/monitors, and the reconfigurable circuit comprises interfaces with the hardware drivers/monitors. **(Figures**

28-30 and their corresponding descriptions)

Regarding Claim 25:

Lin discloses The apparatus according to any one of claims 21 to 24, wherein the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals of different frequencies, the reconfigurable test bench further comprising a clock retrocontrol means operable to in response to a wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal temporarily disable the secondary clock signals with different frequencies from that of the first secondary clock signal. **(Abstract. Figures 1-6, 10, 16, and 67, for example, and their corresponding descriptions. Column 11, Lines 16-35. Column 27, Line 45 – Column 28, Line 57)**

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. All Claims are rejected.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAIF A. ALHIJA whose telephone number is (571)272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

SAA

June 16, 2008